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| 09/801,080 | 03/07/2001 | Natalino Giorgio Busa | NL000133 | 5082 |

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P.O. BOX 3001
BRIARCLIFF MANOR, NY 10510

| EXAMINER | |
|---|---|
| LINDLOF, JOHN M | |

| ART UNIT | PAPER NUMBER |
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| 2183 | |

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**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/801,080 | BUSA ET AL. | |
| | Examiner | Art Unit | |
| | JOHN LINDLOF | 2183 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *15 September 2010*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1 and 3-5* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 and 3-5* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

## DETAILED ACTION

1. Claims 1, 3-5 are presented for examination.

### *Claim Rejections - 35 USC § 112*

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 1, 3-5 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

Independent claim 1, and similarly independent claim 4, contains the limitation "wherein said master controller synchronizes the first functional unit to use output data processed by the second functional unit during the execution of said instruction to provide input data to the second functional unit during the execution of said instruction." This limitation has not been sufficiently described in the specification. The following three sections of the specification are the only locations found to be using the term "synchronization" or any variation thereof:

Page 6, lines 29-31: "This is surely a safe assumption, but allows no **synchronization** between the operations' data consumption and production times and the start time of the other operations in the SFG."

Page 10, lines 20-21: "The effect on the hardware is that the FU might be stalled to better **synchronize** data communicated to and from other operations."

Page 11, lines 10-12: "The complex FU contains its own controller and the only task left to the VLIW controller is to **synchronize** the coarse-grain FU with the rest of the datapath resources."

These sections have been considered in context, and within the scope of the entire specification, however there is still insufficient support for the limitation as claimed. While there is certainly support for the general synchronization of data and for synchronizing a functional unit with other datapath resources, there is insufficient support for the specific synchronization of "the first functional unit to use output data processed by the second functional unit during the execution of said instruction to provide input data to the second functional unit during the execution of said instruction." as claimed.

While other sections of the specification describe providing input and output data to functional units, there does not appear to be any discussion of how this relates to synchronization.

Claims 3 and 5 are rejected for being dependent upon a rejected independent claim.

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 3-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Morikawa et al., US Patent 5,909,565 (hereinafter Morikawa), in view of Mohamed et al., US Patent 6,301,653 (hereinafter Mohamed).

2. As per claim 1, Morikawa teaches:

A data processing device (see e.g. fig. 4), the device comprising: first (see e.g. fig. 4 coprocessor 202) and second (see e.g. fig. 4 data processing unit 207) functional units for performing one or more operations (see e.g. col. 7 lines 1-3, coprocessor and processor instructions), the first functional unit including a slave controller (see e.g. fig. 4 control circuit 210), the one or more operations having a different latency (see e.g. col. 8 lines 6-21, a coprocessor instruction takes more stages than a processor instruction, 4 stages to 2 stages in this example), and a master controller (see e.g. fig. 4 control circuit 205) for controlling a schedule for executing the one or more operations (see e.g. fig. 2 MULQ coprocessor instruction) by the first functional unit (see e.g. col. 16 lines 14-27, a coprocessor instruction executing on the coprocessor is controlled by the processor control during an interrupt), including input/output operations (see e.g. col. 20 lines 8-46, control circuit operations) that are performed by the slave controller of the first functional unit (see e.g. col. 17 line 66 - col. 18 line 21), wherein said master controller

synchronizes (see e.g. fig. 6, data is synchronized using the processor control circuit by transferring data between coprocessor and processor) the first functional unit to use output data processed by the second functional unit during the execution of said instruction (see e.g. fig. 6, data is transferred from the processor to the coprocessor) to provide input data to the second functional unit during the execution of said instruction (see e.g. fig. 6, data is transferred from the coprocessor to the processor).

Morikawa fails to explicitly teach a Very Long Instruction Word (VLIW) architecture for processing VLIW instructions, and performing the one or more operations of an instruction at the same time.

Mohamed teaches a Very Long Instruction Word (VLIW) architecture for processing VLIW instructions (see e.g. col. 2 lines 58-63), and performing one or more operations of an instruction at the same time using shared data during execution of the instruction (see e.g. col. 1 lines 19-56, col. 2, operations/instructions of a VLIW instruction are performed at the same time using shared data).

At the time of the invention it would have been obvious to one of ordinary skill in the art to combine the teachings of Morikawa and Mohamed to use a VLIW architecture, and to perform operations of an instruction at the same time. The processor with coprocessor system of Morikawa teaches the parallel execution of multiple operations, they are merely not disclosed as being a part of a VLIW instruction. There are various advantages to using a VLIW architecture, such as disclosed by Mohamed: "VLIW models are advantageous in that they are very scalable, they are not affected by

'memory wall' concerns, and they save both silicon area and power consumption by off loading the complex instruction scheduling schemes to a compiler."

3. As per claim 3, Morikawa in view of Mohamed teaches:

The data processing device according to claim 1, further comprising halt means controllable by the master controller for suspending operation of the first functional unit (see e.g. col. 16 lines 14-27, the coprocessor execution is halted by a control signal sent by the processor control circuit during an interrupt).

4. Claims 4 and 5 are rejected for reasons corresponding to those given above for claims 1 and 3.

***Response to Arguments***

Applicant's arguments with respect to claims 1, 3-5 have been considered but are moot in view of the new ground(s) of rejection.

***Conclusion***

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JOHN LINDLOF whose telephone number is (571)270-1024. The examiner can normally be reached on Monday-Friday 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Eddie P Chan/
Supervisory Patent Examiner, Art Unit 2183

John Lindlof
(571) 270-1024